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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,865	07/27/2001	Victor Demjanenko	042159.0120	8965

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EXAMINER	
TALAPATRA, ANIKA F	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/916,865	DEMJANENKO ET AL.	
	Examiner	Art Unit	
	Anika F. Talapatra	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/27/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/27/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A (1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Specification

2. The disclosure is objected to because of the following informalities: Background Technology 4, line 6, contains the word "decoder." The correct word in the sentence should be "decoded." Appropriate correction is required.

3. The disclosure is objected to because of the following informalities: Detailed Description 43, lines 14 and 15 lack periods at the end of sentences. Line 14 should read "...$x^8 + x^4 + x^3 + x^2 + 1$." Line 15 should read "...$d_7\alpha^7 + d_6\alpha^6 + \ldots + d_1\alpha + d_0$." Appropriate correction is required.

4. The disclosure is objected to because of the following informalities: Detailed Description 103, lines 6 and 7, refer to incorrect reference numbers in Figure 8. The correct reference numbers are: "The bit error information and the output bit steam are provided *84* to an outer decoder, and the outer decoder produces *86* an information bit stream from the bit error information and the output bit stream." Appropriate correction is required.

Claim Objections

5. a. Claim 6 objected to because of the following informalities: The abbreviation RS is used. Abbreviations are not allowed without first defining the abbreviation in the claims. The claim should read, "...decoder is a Reed-Solomon (RS) decoder." Thereafter, the abbreviation RS can be used in the claims. Appropriate correction is required.

b. Claim 10 objected to because of the following informalities: The abbreviation LDPC is used. Abbreviations are not allowed without first defining the abbreviation in the claims. The claim should read, "...decoder comprises Low-density parity-check (LDPC) decoding." Thereafter, the abbreviation LDPC can be used in the claims. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 rejected under 35 U.S.C. 102(b) as being as being anticipated by Hagenauer et al. (U.S. Patent 5181209) (hereto referred to as Hagenauer). The applicant claims a method for decoding a symbol stream, using an inner soft-output decoder to produce an output bit stream and associated bit error

probabilities; providing to an outer decoder the output bit stream and bit error probabilities; producing an information bit stream by the outer encoder using the output bit stream and bit error probabilities. Hagenauer teaches concatenated decoding, with outer and inner decoders, in which the inner decoder provides soft decisions (i.e. error probabilities) to an outer decoder. These soft decision values are used to produce a corrected output information bit stream (see Hagenauer, column 3 lines 52-66; column 4 lines 1-22 and 65-68; column 5 lines 1-15). This is identical to claim 1.

7. Claim 2 rejected under 35 U.S.C. 102(b) as being as being anticipated by Hagenauer, as applied to claim 1 above. The applicant claims the method in claim 1, with the further limitation that the inner decoder is a Maximum a Posteriori (MAP) decoder. Hagenauer teaches the use of a MAP inner decoder.

8. Claim 6 rejected under 35 U.S.C. 102(b) as being anticipated by Hagenauer, as applied to claim 1 above. The applicant claims the method in claim 1, where the outer decoder is a Reed-Solomon (RS) decoder. Hagenauer teaches that the second or outer decoder may be a RS decoder or other block decoder (see Hagenauer, column 5, lines 40-44). Therefore, it would be obvious to one of ordinary skill in the art that a RS decoder could be used as the outer decoder of claim 1.

9. Claim 7 rejected under 35 U.S.C. 102(b) as being anticipated by Hagenauer, as applied to claim 1. The applicant claims that an outer decoder generates bit error information from bit error probabilities and corrects errors according to bit error information. Hagenauer teaches that the inner decoder generates error probabilities for each symbol. Hagenauer further teaches that the inner decoder provides this information to an outer decoder, and the outer decoder corrects errors in the data stream, based on the error probabilities from the inner decoder (see Hagenauer, column 10, lines 21-44).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Hagenauer, as applied to claim 1 above, further in view of Langhammer et al. (U.S. Patent 6400290) (hereto referred to as Langhammer). The applicant claims the method in claim 1, with the further limitation that the inner decoder is a Logarithmic MAP (LOGMAP) decoder. Hagenauer does not teach the use of a LOGMAP decoder. Langhammer teaches the use of a LOGMAP decoder in a concatenated system. The use of a LOGMAP decoder reduces the number of logic levels required, while maintaining performance near the Shannon error limit (see Langhammer, column 1 lines 32-49 and column 2 lines 49-53). Therefore, it would be obvious to one of ordinary skill in the art that a LOGMAP decoder could be used as the inner decoder of claim 1.

11. Claim 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Hagenauer, as applied to claim 1 above, in view of Gueguen et al. (U.S. Patent Application 2001/0039638) (hereto referred to as Gueguen). The applicant claims the method in claim 1, with the further limitation that the inner decoder is a

Maximum LOGMAP (MAXLOGMAP) decoder. Hagenauer does not teach the use of a MAXLOGMAP decoder. Gueguen teaches the use of a MAXLOGMAP decoder in a concatenated system (see Gueguen, page 1 paragraph 7). The use of a MAXLOGMAP decoder may improve performance to be nearer to the Shannon error limit. Therefore, it would be obvious to one of ordinary skill in the art that a MAXLOGMAP decoder could be used as the inner decoder of claim 1.

12. Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Hagenauer, as applied to claim 1 above. The applicant claims the method in claim 1, with the further limitation that the inner decoder is a soft-output Viterbi Algorithm (SOVA) decoder. Hagenauer does not teach the use of a SOVA decoder. However, it is known in the art that SOVA decoders can calculate bit error probabilities of a data stream. Therefore, it would be obvious to one of ordinary skill in the art that a SOVA decoder could be used as the inner decoder of claim 1.

13. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Hagenauer, as applied to claim 1, further in view of Barazeche et al. (U.S. Patent 4577309) (hereto referred to as Barazeche). The applicant claims that bit error information is generated by subjecting bit error probabilities to a thresholding procedure. Hagenauer does not teach the use of a thresholding procedure to generate bit error information. Barazeche teaches the use of threshold, where there is thus a variable threshold which adapts to the noise level in the transmission medium and thereby gives a fixed error probability, whereas with a fixed threshold the error probability would depend on the transmission level. (see Barazeche, Detailed Description, 33). It would be obvious to one of ordinary skill in the art to use thresholding for determining bit error information from bit error probabilities.

14. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Sun (Introduction to Low density parity check codes) (hereto referred to as Sun), in view of Wadayama (web page, Introduction to Low density parity check codes and Sum-Product Algorithm) (hereto referred to as Wadayama) and further in view of Wang et al. (IEEE, Vol. 42, No. 2, March 1996) (hereto referred to as Wang). The applicant claims a method for decoding a symbol stream, using an inner sum-product decoder to produce an output bit stream and associated bit error probabilities; providing to an outer decoder the output bit stream and bit error probabilities; producing an information bit stream by the outer encoder us
15. ing the output bit stream and bit error probabilities. Wadayama and Sun teach Low-density parity-check (LDPC) decoding, which uses the sum-product algorithm. Using the sum-product algorithm, a LDPC decoder is capable of calculating bit error information that indicates which outputted decoded bits have errors. This is identical to the first second, and fourth elements of the applicant's claim 9.

In the third element of claim 9, the applicant claims that the inner decoder provides to an outer decoder the output bit stream and bit error probabilities. Wadayama and Sun do not explicitly teach that an inner decoder provides information to an outer encoder. Wang teaches a soft-output decoding algorithm for concatenated systems, where an inner decoder provides probability of error to an outer decoder (see Wang, Introduction and Metrics for Generalized Soft Decision Decoding). It is well known in the art that using multiple decoders, linked by an interleaver, also known as using concatenated decoding, can narrow the gap to the theoretical Shannon error limit. Therefore it would be obvious to one of ordinary skill in the art that soft information, computed by the inner decoder, be provided from the inner decoder to an outer decoder so that the decoders are used together in a concatenated or iterative system.

16. Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Sun in view of Wadayama and further in view of Wang, as applied to claim 9. The

applicant claims sum-product decoding comprises LDPC decoding. Wadayama teaches that LDPC codes are computed using the sum-product algorithm. It is well known in the art that LDPC decoding may narrow the gap to the theoretical Shannon error limit. Therefore it would be obvious to one of ordinary skill in the art that sum-product decoding comprises LDPC encoding.

17. Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Sun in view of Wadayama and further in view of Wang, as applied to claim 9. The applicant claims the method in claim 9, with the further limitation that the outer encoder is a RS decoder. Sun, Wadayama, and Wang do not teach the use of an outer RS decoder. However, it is known in the art that RS decoders can be used as inner or outer decoders in a concatenated decoder system. It is well known in the art that a RS outer decoder may narrow the gap to the theoretical Shannon error limit. Therefore, it would be obvious to one of ordinary skill in the art that a RS decoder could be used as the outer decoder of claim 9.

18. Claim 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Sun in view of Wadayama and further in view of Wang, as applied to claim 9. Claim 12 is rejected on the same basis as claim 9. In claim 12, the applicant claims correcting errors using bit error information producing an information bit stream. Using bit error probabilities to correct errors and produce a corrected information bit stream was rejected in number 13 above.

19. Claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Wadayama. The applicant claims an outer and an inner encoder where the outer encoder provides an ouput bit stream to the inner encoder, and the inner encoder encodes the bit stream using the sum-product algorithm. Wadayama teaches that LDPC codes were first invented in by Gallager in 1962, and that LDPC codes are computed using the sum-product algorithm. Wadayama does not teach the use of LDPC codes with an outer encoder. It is known in the art that

LDPC codes are typically used alone, without a second encoder. However, it is known in the art that often systems comprise two or more encoders. Therefore it would be obvious to one of ordinary skill in the art to use an outer encoder in addition to the LDPC encoder.

20. Claim 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Wadayama, as applied to claim 13 above. The applicant claims the method in claim 13, with the further limitation that the outer encoder is a RS encoder. Wadayama does not teach the use of an outer RS encoder. However, it is known in the art that often systems comprise two or more encoders. It would be obvious to one of ordinary skill in the art that an outer RS encoder be used in addition to the LDPC encoder, so as to protect against burst errors.

21. Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Wadayama. The applicant claims sum-product encoding which comprises LDPC encoding. Wadayama teaches that LDPC codes are computed using the sum-product algorithm. Therefore it would be obvious to one of ordinary skill in the art that sum-product encoding comprises LDPC encoding.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anika F. Talapatra whose telephone number is 571-272-6039. The examiner can normally be reached on 08:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M. G

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER